Cargo-culting an SBCL backend

Charles Zhang

December 20, 2019
1. Introduction

2. Writing a new backend

3. Current status

4. Future backend work
Who am I?

Third year undergraduate student
Linguistics & Math
Research interest: Historical Linguistics
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What is RISC-V?

New CPU architecture spawned by UC Berkeley

Original purpose was as a teaching language

A descendant of the original RISC architectures

Whence came MIPS as well, the previous teaching language

Fixed some antiquated design decisions

No branch delay slots

Explicitly open-source, libre, patent-free ISA.

Extensible

Specifications for various ISA extensions modular, base ISA is tiny

A lot of hype and gaining corporate support

Potential uses range from embedded to general purpose (one can hope!)

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Why SBCL + RISC-V?

Intro machine structures course last fall semester
C, RISC-V assembly, CPU architecture (cache, virtual memory etc.)
Final project was implementing a RISC-V CPU in a visual HDL.
Upshot: Had to learn every base ISA instruction, its encoding, and how to implement it in hardware

Christophe Rhodes’s blog post about SBCL + RISC-V on trains.
I like SBCL.
The time was ripe.
Or was it?
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Really important
I had no hardware, only a (broken) slow Fedora qemu VM.

cold init initially took about 30 minutes.

warm load added another half hour.

don't get me started on the test suite.

Turns out this porting effort was very premature.

no GDB :(

broken kernel :(

Real Linux-capable SiFive board: $1000+ :((
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Christophe started the port as a 32-bit port. So I continued developing it as a 32-bit port. Later, found out only RV64 is Linux-capable at the moment. Oops. Upshot: Now the only shared {32/64}-bit backend in SBCL. It helps that RV32 and RV64 were designed at the same time.
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Write the instruction definitions

Christophe defined a good deal of the base ISA instructions. Good macros help! The regularity of the instruction set is a boon. Adding RV64 support later was easy. Needed to implement:

- Labels and addressing modes
- Relocations
- Floating point instructions (F and D extensions)
- CSR frobbers
- Pseudoinstructions
- `define-instruction-macro`
- Load 64-bit Immediate on RV64 - what a doozy!

Adding special cases reduced core size in half. Even the LLVM backend does a worse job.
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Read the CMUCL docs, especially the internals guide by Rob MacLachlan. Nothing in the SBCL tree comes close.

Read Alastair Bridgewater's ARM port logs.

Read the source judicially.

Get schooled on IRC.

I'm karlosz on freenode.

In the end, none of this really matters that much though. Just cargo-culting until you understand.

Comment in local.lisp

;;;; Note: Take a look at the compiler-overview.tex section on "Hairy function representation" before you seriously mess with this stuff.

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(defreg zero 0) (defreg lr 1)
(defreg nsp 2) (defreg global 3)
(defreg thread 4) (defreg lra 5); alternate link register
(defreg cfp 6) (defreg ocfp 7)
(defreg nfp 8) (defreg csp 9)
(defreg a0 10) (defreg nl0 11)
(defreg a1 12) (defreg nl1 13)
(defreg a2 14) (defreg nl2 15)
...
(defreg cfunc 26) (defreg lexenv 27)
(defreg null 28) (defreg code 29)
(defreg lip 30) (defreg nargs 31)

(defregset descriptor-regs a0 a1 ... l2 l3 ocfp lra lexenv)
(defregset boxed-regs a0 a1 ... l1 l2 l3 ocfp lra lexenv code)
(define-argument-register-set a0 a1 a2 a3)
Write VOPs

VOPs are the translators ("templates") that turn backend independent "virtual machine" instructions into native code. Read every backend's version for inspiration on how to do it best. A good way to understand what the IR2 instructions do in the first place.

MIPS is architecturally close to RISC-V.
ARM64 and x86-64 have the cool new optimizations.
PPC somewhere between MIPS and ARM.

Mostly blindly copy and hope it works. The calling convention VOPs are the most design-heavy for a new CPU and least amenable to cargo culting. Good opportunity to use the ISA to its fullest extent.

Try and microoptimize every VOP. It's quite satisfying to shave off a few bytes here and there. Dealing with some 64-bit differences in object layout and tagging extremely annoying.
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Runtime glue

Implement some assembly routines

Write operating system support

Signal handling, FP handling, and the like

GC hookup

call_into_lisp

and

call_into_c

usually part of a .S file.

Decided to write it in the Lisp assembler rather than the system assembler, the first backend to do so

Have full power of Lisp to generate assembly.
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Bootstrap time

OK. Now you've cross-compiled a cold core and have a runtime to run it. Start it in the VM. Lose instantly. Debug, fix, repeat. Anything bad can happen, especially early in cold-init. Illegal instructions, smashed interrupt stacks, off by one errors, bad VOPs, bad instruction encoding, bad runtime glue... Good luck finding out why. GDB will show you the way.

I had no GDB. Write out trace files and manually disassemble cores, step through the instructions manually like it's 1962. Hope you didn't smash the stack too hard and corrupt LDB so you can at least read out the registers at crash time. It gets better once you get a Lisp debugger.
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It gets better once you get a Lisp debugger.
OK. Now you’ve cross-compiled a cold core and have a runtime to run it.

Start it in the VM. Lose instantly.

Debug, fix, repeat.

*Anything* bad can happen, especially early in cold-init.

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- Good luck finding out why.

GDB will show you the way.
Bootstrap time

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The big bad

In late March I hit a big snag which crippled the porting effort. A signal routine related to sigmask handling in the runtime would always fail. After much chasing, turned out to be a kernel bug. By then there were new Fedora images, with GDB and a working signal library. Phillip Matthias Schäfer wanted to try the port and had the same crashes. Indeed he was using the broken VM image. Later he ported sb-rotate-byte support to RISC-V.
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Later he ported `sb-rotate-byte` support to RISC-V.
Initially started with cheneygc. Christophe expressed it would probably be easier to start off this way. Got a real core with cheneygc eventually. After pestering on IRC I ported to gengc. Much faster. cheneygc has some issues on 64-bit platforms. Defaults to gengc now, though technically cheneygc should still work with no problem.
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Current status

Can run quicklisp.
Supports `sb-linkage-table`.
Supports some stack allocation.
Only a few test suite failures remaining mostly to do with floating point issues.
RISC-V doesn't have hardware floating point traps.
Much work has been done on optimizing the VOPs and finding a good calling convention.
Works for at least one other person on a good qemu image.
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What’s left for RISC-V?

C extension

Potential for big space savings.

Unclear what the right way to codegen this is.

Have instruction emitters choose C-insts AND/OR...

Write versions of VOPs using C-insts.

Alien callbacks

Better DX handling

Debugger stuffs

Single stepping

Native threading

Need to understand the RISC-V concurrency model.

Need to settle on a synchronization method.

AFAICT these specs are still in flux anyway.

Jump tables!

Leverage Douglas Katzman and Stas Boukarev’s efforts on some new IR2 machinery in the backend.

Includes peephole optimizations and case dispatch =] jump table work.

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  - array getter/setter and floating point VOPs especially.
- More code sharing, maintainability
  - Don't want to have to make two sets of identical changes to the 32-bit ports and 64-bit ports living in different directories.
  - Looking at you, PPC and PPC64.
- Adding C runtime support could be easier.
- Our hookup of GC into backend codegen and runtime is too complicated.
  - We support two GCs, but in an ad-hoc manner.
  - gengc on older backends seems doable.
- Make threads, alien callbacks, gengc etc. less tedious to implement.
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